Modeling and Analysis of Duty Cycle Mode Voltage Ringings in Wireless Power Transfer Systems

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***Abstract*—Wireless power transfer system in commercial electronic devices often employ duty cycle control for enhanced load regulation capabilities. When the transmitter operates in deep duty cycle mode, e.g. under light load conditions, power receivers based on synchronous rectifiers can exhibit significant voltage ringings on the ac nodes. For receiver-side in-band communication demodulation (e.g. frequency-shift keying as regulated in WPC Qi standards), these transient ringings can be particularly concerning as they can cause data decoding errors, resulting in frequent charging disruptions. While there is a clear need to better understand the ac ringing patterns, most existing literature provide sets of transcendental equations that have no easy analytical solutions. This paper introduces a modeling approach for ringings in duty cycle mode, together with the simplifying assumptions that allow derivations of the ringing waveform without overly complex timing analysis. Good matching is achieved between the analytical predictions, circuit simulations, and experimental results. The proposed method enables highlighting of likely problematic operating scenarios for enhanced in-band communication robustness.**

***Index Terms*—Wireless Power Transfer, LLC Converters, Qi, In-Band Communication, Frequency-Shift Keying, Time-Domain Analysis**

I. Introduction

The power transmitters in inductive wireless power transfer (WPT) systems, for example in consumer electronic devices, often employ duty-cycle control to gain more flexible power regulation capabilities than achievable with bridge voltage and/or frequency control alone [1]–[5]. While the system is operating under duty-cycle mode, the transmitter (Tx) switching frequency and inverter bridge voltage are typically fixed, while the magnitude of the fundamental ac voltage component generated by the Tx is varied by controlling the on-time of each inverter switch. An example WPT system power stage and duty-cycle mode control pattern are shown in Figs. 1 and 2 respectively. Depending on the system configuration and initial conditions, during the Tx "zero" time, marked as t_1 to t_2, noticeable voltage oscillations on receiver (Rx) ac nodes $V_{ac1,2}$ can appear. This behavior may cause several adverse effects such as distortion of in-band communication data decoding, regulated by the Wireless Power Consortium (WPC) Qi-specfication, which can lead to power transfer disruptions such as disconnections due to mis-decoded packets [6], and potential mis-firings of the synchronous rectifier [7], with efficiency and reliability implications.

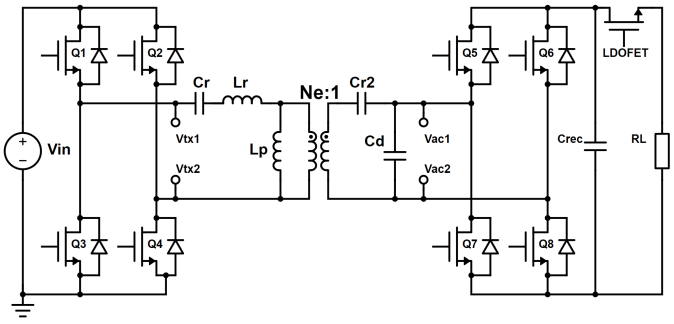

Fig. 1. An example WPT system power stage with Tx inverter and Rx rectifier in full-bridge and an "L"-model representing coupled coils.

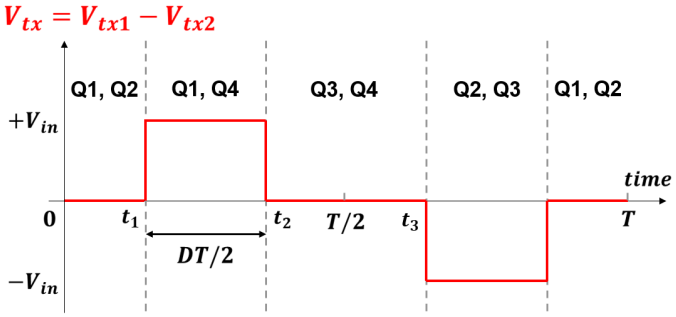

Fig. 2. Tx duty cycle mode operation. Same V_{tx} waveform can be achieved with Tx phase-shifts.

The time and frequency domain behaviors of the LLC converter, whose power stage is analogous to the wireless power transfer (WPT) system examined in this paper, have been thoroughly investigated in the literature [8]–[12]. However, few insights can be gained towards WPT performance enhancements as the equation set describing the transient voltages is often transcendental, with nested inter-dependencies and no easy analytical or numerical solutions. This paper presents a modeling technique for voltage oscillations that incorporates simplifying assumptions to address the derivation

of crucial initial conditions and the distinctions between LLC and WPT systems. The rest of the paper is organized as follows: Section II reviews a common FSK in-band communication decoding mechanism and the underlying root cause of decoding failures caused by ac voltage ringings, while Section III presents the proposed duty-cycle mode ringing model and circuit analysis techniques. Modeling, simulation, and experimental results are discussed in Section IV, and a conclusion is drawn in Section V.

II. FSK Communication Mechanism

This section introduces the WPC Qi frequency-shift keying (FSK) in-band communication mechanism, and the data packet decoding errors induced by ac voltage ringings.

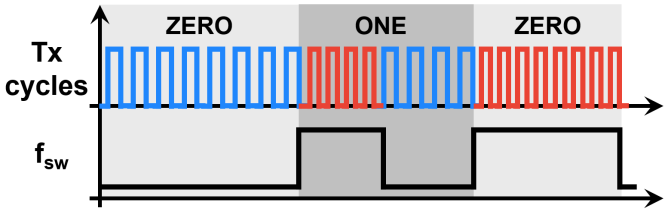

Fig. 3. A simplifying illustration of the bi-phase frequency-shift-keying data encoding scheme. The Tx sends out encoded data bits by shifting between two slightly different operating frequencies. A data bit zero is encoded by keeping the same switching frequency for a certain period (e.g. 512 cycles), and a data bit one is encoded by changing frequency in the middle of the period (e.g. 256 cycles at high frequency, followed by 256 cycles at low frequency). The Rx decodes the data bits by detecting such frequency changes.

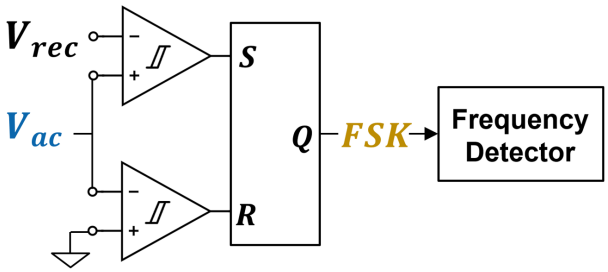

Fig. 4. A common FSK decode mechanism in WPT receivers. The voltage comparators compare ac node voltage (e.g. V_{ac1}) and rectified dc voltage (e.g. V_{rec}), and the output is routed to an S-R latch to generate edges synchronous to transmitter switching frequency (denoted FSK) for frequency modulation detection.

Wireless Power Consortium's Qi spec mandates Tx-to-Rx in-band communication in the form of differential bi-phase FSK encoding. During power transfer, the Tx perturbs its switching frequency for a number of ac cycles and then reverts back, and uses the perturbation pattern to encode data bits [6]. A FSK data encoding mechanism example is illustrated in Fig. 3. The Tx sends a message bit zero by keeping its operating frequency constant for a fixed duration (e.g. 512 continuous cycles), and sends a bit one by perturbing its frequency in the middle of duration (e.g. 256 cycles at perturbed frequency and 256 cycles at original frequency). These perturbations continue until a complete data packet is sent out. The Rx needs to properly detect these frequency change patterns and decode the message bits to stay in power transfer phase. The frequency perturbation polarity and depth are negotiated between Tx and Rx at the beginning of a charging session.

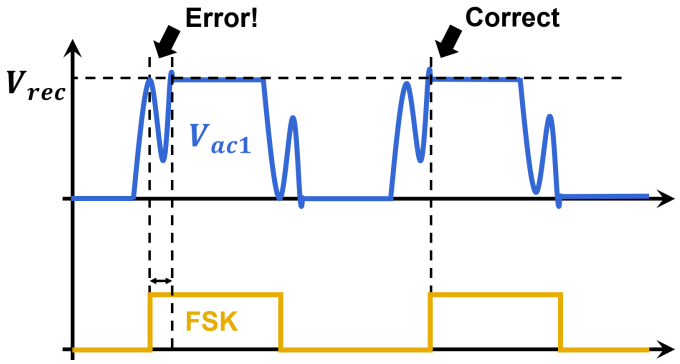

Fig. 5. A waveform showing how ac voltage ringings can lead to decoding errors. Usually V_{ac1} reaches V_{rec} only when the rectifier starts conducting, however, if the transmitter operates in deep duty-cycle mode, large ac ringings can occur on the ac nodes. This may cause the $V_{rec} - V_{ac1}$ comparator to trigger early and to erroneously set the FSK signal edge. This can introduce a significant timing error when counting the cycle durations, and thereafter result in errors in FSK communication decoding.

To decode the FSK message, the Rx typically senses the duration of each ac cycle, and periodically counts and compares the total duration of these ac cycles. Fig. 4 shows a common decoding mechanism based on voltage comparators and a SR-latch, and each rising edge of the "FSK" signal represents a new switching cycle. The digital frequency detector then processes this signal to determine the frequency change pattern and decoded message bits. The timing interval between the "FSK" edges is a critical factor since it directly impacts frequency detection results.

However, when the Tx operates in deep duty cycle mode, e.g. under light load conditions, the Rx ac nodes can see large ac voltage ringings, as shown in Fig. 5. The ac node ringings can cause mis-triggering of the comparators, and hence wrong timing of the "FSK" signal rising edges. This can confuse the frequency detector as an extra time period is included in the interval, and in turn lead to decoding errors, data packet losses, and power transfer disruptions.

The decoding errors occur most frequently when the peak ac ringings are hovering near V_{rec}, in other words, when the comparator triggers inconsistently. In other words, if the ringing amplitude is so large that the comparator always triggers at the "error" markings, the "FSK" edge intervals still correctly reflect Tx switching frequency. It is the irregularities in the "FSK" edges that induce communication errors. The rest of the paper discusses the modeling of the ac ringings, with a focus on identifying the problematic ringing patterns.

III. Simplified Duty Cycle Mode Model

This section introduces the simplified duty cycle mode ac ringing model and associated assumptions. As shown in Fig. 6, inspired by the LLC converter frequency mode analysis

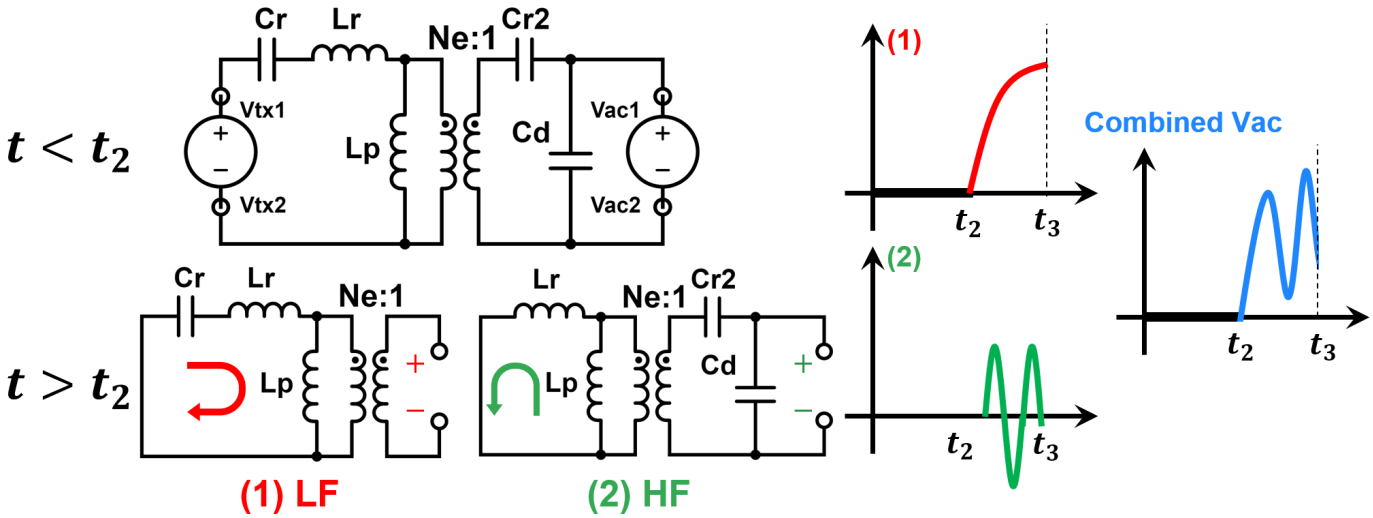

Fig. 6. Equivalent WPT circuits at stage 1 (top half, $t < t_2$) and stage 2 (bottom half, $t > t_2$) of the duty cycle mode transient model. During stage 1, both the Tx inverter and Rx rectifier are conducting and set a fixed voltage at the respective terminals. During stage 2, we separate the linear circuit into both low-frequency (LF) components where the series C_r-L_r-L_p resonance dominates, and the high-frequency (HF) components where the large C_r is treated as short, and the parallel resonance occurs between L_r, L_p and the series C_d-C_{r2} reflected across the transformer. These two resonance behaviors are separately analyzed and then super-imposed together at the V_{ac} nodes to form the ac ringing voltage transients.

approach in [8], we separate WPT duty cycle mode operation into two stages: (1) Rx rectifier on (t_1 to t_2), and (2) Rx rectifier off / ringing begins (t_2 onward). We assume the rectifier conduction is synchronized with the Tx inverter in this scenario, so the time instances ($t_{1,2}$) match with those shown in Fig. 2. In stage 1, dc voltage at V_{tx}, V_{ac} ports are known and we derive the important initial conditions for stage 2. In stage 2, V_{tx} is shorted and V_{ac} is open, and we further divide the linear circuit into low-frequency and high-frequency components, solve them separately, and recombine for the eventual ac transient waveform. A key end result of the model is how close peak V_{ac} can be with respect to V_{rec} before the rectifier conducts again at t_3.

A. Stage 1 - Setting Initial Conditions

Stage 1 refers to the period where both Tx inverter and Rx rectifier are conducting. In this stage, we first presume the voltage across Tx resonant capacitor C_r is primarily sinusoidal, and hence the resonant current can be expressed as in (1), where $\omega_s = 2\pi f_{sw}$ is the angular switching frequency, and A and ϕ are the unknown magnitude and phase (with respect to $V_{tx}(t)$).

$$I_{C_r}(t) \approx A \cdot \sin(\omega_s t + \phi) \tag{1}$$

As a next step, leveraging first-harmonic approximation and power conservation, we have the relationship in (2), where $V_{fund,\,rms}$ and $I_{C_r,\,rms}$ are the rms values of the V_{tx} fundamental component and I_{C_r} respectively. We made a distinction between V_{rec}, the dc voltage after the Rx rectifier, and V_{out}, the output voltage across load resistor R_L, to account for the potential headroom variations from the LDO. Given a steady operating condition, all parameters except the magnitude and phase of I_{C_r} are known.

$$\begin{aligned} P_{in} &\approx V_{fund,\,rms} \cdot I_{C_r,\,rms} \cdot \cos(\phi) \\ &= P_{out} \approx V_{rec} \cdot V_{out} \,/\, R_L \end{aligned} \tag{2}$$

In addition, as the Rx load current is usually small under duty cycle mode, we further assume little discrepancy exists between the inductor currents I_{L_r} and I_{L_p}, at the beginning and end of stage 1 (at the time instances t_1 and t_2), as expressed in (3). The current change in L_p during stage 1, ΔI_{L_p}, is denoted on the left as an integral, and the current change in I_{C_r}, ΔI_{C_r}, is expressed on the right.

$$\begin{aligned} \Delta I_{L_p} &= \int_{t_1}^{t_2} (V_{rec} + V_{C_{r2}}(t) \cdot N_e)\, dt \,/\, L_p \\ &\approx \Delta I_{C_r} = I_{C_r}(t_2) - I_{C_r}(t_1) \end{aligned} \tag{3}$$

A further simplification is made regarding the typically large Rx-side resonant capacitor C_{r2} during stage 1, that in periodic steady-state operation, it is charged linearly from $-V_{pk}$ to V_{pk}. Therefore, the effect of $V_{C_{r2}}(t)$ on the inductor L_p current change during stage 1 can be mostly neglected.

These assumptions enable a much-simplified solution to $I_{C_r}(t)$ during stage 1, obtainable through numerically solving the set of two equations in (4), where D is the duty cycle. This allows us to capture the Tx resonant tank current profile $I_{C_r(t)}$. By plugging in the time instance t_2 into this solution, the initial conditions for the LF/HF circuits and the ac ringing waveform during stage 2 can be derived.

$$\begin{cases} -2A\omega_s C_{r1} \cos(\phi) \sin(\dfrac{D\pi}{2}) = \dfrac{D \cdot N_e \cdot V_{rec}}{2 f_{sw} \cdot L_b} & \text{(4a)} \\ -4A f_{sw} C_{r1} V_{in} \sin(\phi) \sin(\dfrac{D\pi}{2}) = \dfrac{V_{rec} \cdot V_{out}}{R_L} & \text{(4b)} \end{cases}$$

B. Stage 2 - Superimposing LF/HF circuits

The ac ringings happen during stage 2, where the Tx inverter enters "zero" mode with $V_{tx} = 0$, and the Rx rectifier stops conducting as $V_{ac1} - V_{ac2} < V_{rec}$. To simplify the analysis of the fifth-order resonant circuit, we separate the linear circuit by frequency range and combine the solutions to model the ac ringing behavior.

As can be observed from Fig. 6, in stage 2 the Rx-side resonant capacitance C_{r2} does not participate in the LF resonance since the Tx-side capacitor C_r and inductances $L_r + L_p$ dominate the LF resonance. In addition, given the typically large Rx-side resonant capacitance C_{r2}, it's effectively an ac short during HF resonance. Therefore, we introduce a simplifying assumption that the voltage across C_{r2} during stage 2 remains relatively stable (at V_{pk}), and we approximate V_{pk} in (5) by finding the total output charge delivered through C_{r2}. The voltage across C_{r2} introduces a dc offset, and impacts the magnitude of the HF ac ringing voltage at nodes $V_{ac1,2}$.

$$V_{pk} \approx \frac{Q_{out}}{2 \cdot C_{r2}} \approx (V_{out} \cdot T)/(4 \cdot R_L \cdot C_{r2}) + V_{rec} \cdot C_d / C_{r2} \quad (5)$$

Following a similar analysis procedure outlined in [8], [9], and leveraging the initial conditions parameters A and ϕ numerically solved from (4), the LF component of the ringing voltage referred to Rx ground, $V_{ac,LF}(t)$ can be expressed as in (6).

Ensuring the super-imposed LF and HF components match with the initial conditions, e.g. as described in (7), the HF component of the Rx ground-referred ringing voltage, $V_{ac,HF}(t)$ can be derived as in (8).

$$V_{ac,LF}(t - t_2) = \frac{V_{rec}}{2} - \frac{L_p}{2N_e(L_r + L_p)} A \sin(\omega_s(t + \frac{1+D}{4f_{sw}}) + \phi) \quad (6)$$

$$V_{ac,LF}|_{t=t_2} + V_{ac,HF}|_{t=t_2} = V_{rec} \quad (7)$$

$$V_{ac,HF}(t - t_2) = (\frac{V_{rec} + V_{pk}}{2} + \frac{L_p}{2N_e(L_r + L_p)} A \sin(\frac{(1+D)\pi}{2} + \phi)) \times \cos(\frac{t}{\sqrt{\frac{L_r L_p}{N_e^2(L_r + L_p)} \cdot \frac{C_{r2} \cdot C_d}{C_{r2} + C_d}}}) - \frac{V_{pk}}{2} \quad (8)$$

$$V_{ac}(t) = V_{ac,LF}(t) + V_{ac,HF}(t) \quad (9)$$

Thus, compounding the LF and HF components together, the overall ac ringing voltage during stage 2 is dubbed by (9).

IV. Results and Discussions

Leveraging the modeling approach in Section III, a series of analytical ac ringing waveforms is derived and compared with simulation results. Further, a two-dimensional sweep over duty cycle (D) and load (R_L) are conducted to highlight potentially problematic operating scenarios, and experimental verifications are conducted at identified operating points.

A set of analytical and circuit simulation models, with parameters listed in Table I, are built using MathCAD and LTSpice. The modeled and simulated transient V_{ac} ringing waveforms are plotted and compared in Fig. 7, with good matching over the Rx-side dead-time duration from t_2 to t_3.

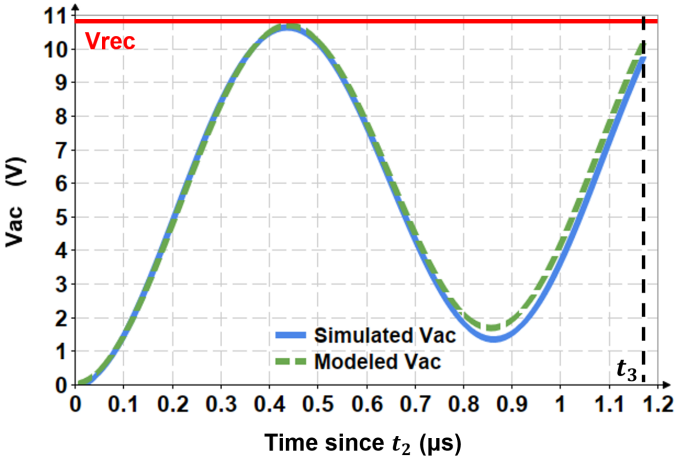

Fig. 7. Modeled and simulated Rx-ground-referenced V_{ac} ringing waveforms. The starting time from the circuit simulation result and the model is aligned to be both at $t = t_2$. Good alignment between the simulated and modeled results can be observed, and in this operating scenario, the peak ringing voltage is very close to V_{rec}, a behavior prone to inducing FSK decoding errors.

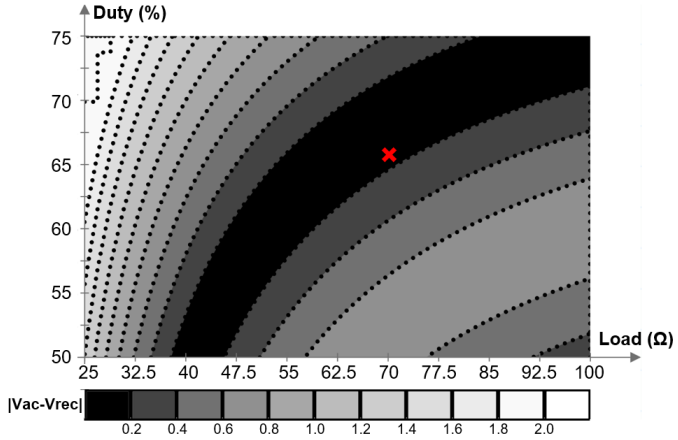

Fig. 8. A contour map of minimum $|V_{ac} - V_{rec}|$, with fixed WLC setup and 2-D sweep over different Tx operating conditions (duty cycle D) and Rx loads (load R_L). The darker regions indicate a higher likelihood of FSK decode errors. The location marked by a red cross is simulated and compared with the model prediction.

Further, leveraging the low-overhead analytical model, which requires numerically solving only the two equations in (4), a sweep of the minimal $|V_{ac} - V_{rec}|$ is conducted over operating ranges, as shown in Fig. 8. This plot exhibits the likelihood of the FSK voltage comparator mis-triggering over the swept conditions in deep duty cycle mode and highlights the regions where special attention to in-band communication decoding errors is warranted.

TABLE I
PARAMETERS USED IN MODELING, SIMULATION, AND EXPERIMENTAL VALIDATION.

C_r	L_r	L_p	N_e	C_{r2}	C_d	V_{in}	V_{rec}	V_{out}	f_{sw}	D*	R_L*
250 nF	7.07 uH	7.35 uH	0.797	400 nF	3.3 nF	12 V	10.8 V	10 V	145 kHz	66%	70 Ω

*: May vary at different WLC system operating points.

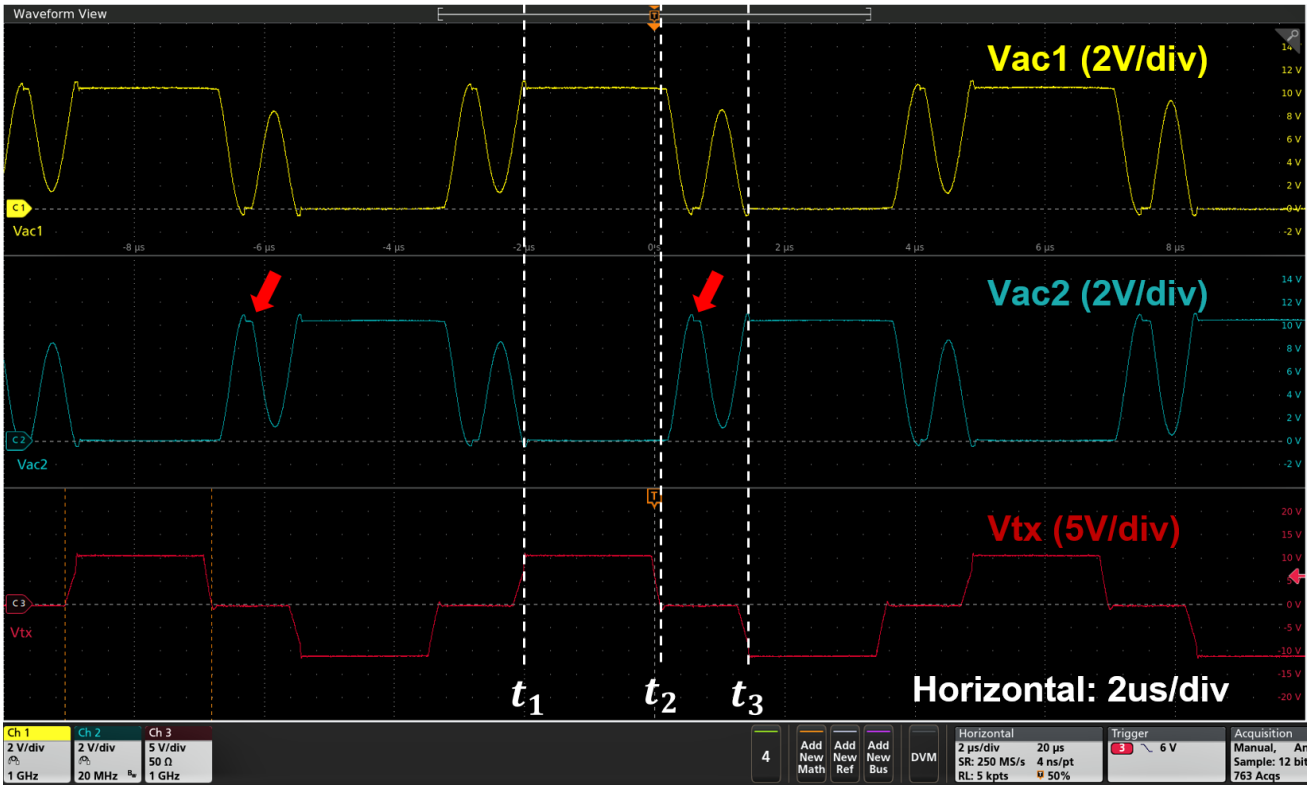

Fig. 9. Annotated experimental results with Tx inverter waveforms V_{tx} and Rx ac ringing waveforms $V_{ac1,2}$. The timing instances t_{1-3} are overlayed with the waveform, and it can be observed that the Tx inverter "zero" phase is aligned with Rx rectifier off phase as expected. The red arrows mark the instances where V_{ac2} rises close to V_{rec}, as indicated by the model and contour sweeps.

The system operating point of Fig. 7 is marked with a red cross in Fig. 8. Here the model predicts a voltage headroom of only 0.114 V from V_{rec}, while the SPICE simulation yields 0.176 V, which means this scenario has high chances of V_{ac} touching V_{rec} and falsely triggering the comparator.

To validate the analytical and simulation results, an experimental setup is constructed with the same parameters in Table I, except R_L is replaced with a constant current load. A photo of the setup is shown in Fig. 10.

The Tx inverter bridge voltage V_{tx}, and the ac node voltages $V_{ac1,2}$ are captured and plotted together with annotations in Fig. 9. It can be observed that the Tx inverter on-time (t_1-t_2) and off-time (t_2-t_3) roughly correspond with the Rx rectifier conduction-time and dead-time, validating the synchronization assumption in Section III. Further, slight V_{ac} ringing overshoots touching V_{rec} (i.e. a "flatness" due to rectifier body-diode conduction) can be seen as marked by the red arrows, confirming the heightened communication decoding error risks.

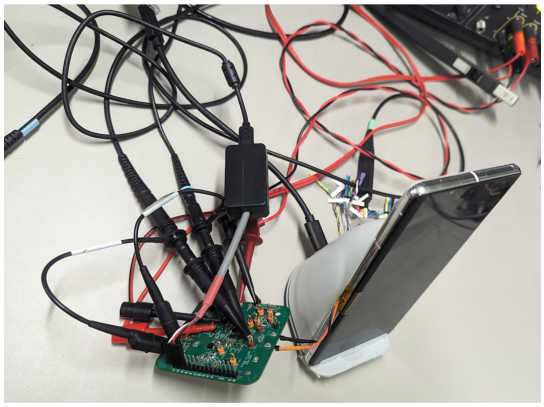

Fig. 10. The experimental setup for Tx bridge voltage and Rx $V_{ac1,2}$ measurements. The Tx is a wireless charging stand, with a differential probe on $V_{tx1,2}$ respectively. The Rx system consists of the receiver coil from a phone with the coil wired out, and the rectifier IC mounted on an evaluation kit. A constant current load, effectively simulating the load resistor, is applied at the dc side of the Rx rectifier.

V. Conclusion

This paper discusses a simplified modeling and analysis approach for transient ac voltage ringings, commonly present in wireless power transfer systems operating in duty cycle mode. The model provides design insights for enhancing Qi regulated FSK in-band communication decoding robustness, and highlights potentially problematic cases with low numerical solution overhead. The model aligns well with simulated results, and the experimental results further validate the simplifying assumptions and model predictions.

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